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IN THE CLAIMS

1. (Currently Amended) A synchronous Flash memory device comprising:
a memory array;
a control circuit; and
a synchronous memory interface, wherein the synchronous Flash memory device begins an iterating process ~~initialization cycle~~ upon receiving a power signal on a power bus, and stops the iterating process ~~initialization cycle~~ upon receiving an external electronic command, and where the iterating process iterates at least twice and performs an initialization cycle of the synchronous Flash memory device during each iteration.

2. (Currently Amended) The synchronous Flash memory device of claim 1, wherein the external electronic command is received through the synchronous interface.

3. (Currently Amended) The synchronous Flash memory device of claim 2, wherein the external electronic command is an SDRAM compatible "STOP" command.

4. (original) The synchronous Flash memory device of claim 1, wherein the synchronous interface is an SDRAM or a DDR-SDRAM compatible interface.

5. (Currently Amended) The synchronous Flash memory device of claim 1, wherein the iterating process of repeating initialization cycles begins when the power signal on the power bus reaches a predefined trip point.

6. (Currently Amended) The synchronous Flash memory device of claim 1, wherein the iterating process of repeating initialization cycles begins a predefined time period after receiving the power signal on the power bus.

7. (Currently Amended) The synchronous Flash memory device of claim 1, wherein the iterating process of repeating initialization cycles stops at a random point in the currently executing ~~iterating~~ initialization cycle when the external electronic command is received.

8. (Currently Amended) A memory device comprising:
a memory array;
a control circuit; and
a memory interface, wherein the memory device commences a continuously looping ~~initialization~~ cycle upon receiving a power signal, and stops the continuously looping ~~initialization~~ cycle upon receiving an external system signal, and where the continuously looping cycle loops at least twice and performs an initialization of the memory device during each loop.

9. (original) The memory device of claim 8, wherein the memory device is a non-volatile memory device.

10. (original) The memory device of claim 8, wherein the memory device is a synchronous Flash memory device.

11. (original) The memory device of claim 8, wherein the memory interface is a synchronous memory interface.

12. (Currently Amended) The memory device of claim 8, wherein the continuously looping ~~initialization~~ cycle commences when the power signal reaches an identified level.

13. (Currently Amended) The memory device of claim 8, wherein the continuously looping ~~initialization~~ cycle commences a predefined time period after receiving the power signal.

14. (Currently Amended) The memory device of claim 8, wherein the continuously looping ~~initialization~~ cycle completes at a random point in the ~~continuously looping~~ initialization ~~cycle~~ when the external system signal is received.

15. (Currently Amended) A synchronous Flash memory device comprising:

a memory array;

a control circuit; and

a synchronous SDRAM compatible memory interface, wherein the synchronous Flash memory device begins a continuously looping ~~initialization~~ cycle upon a power signal on a power bus reaching a specified trip point, and stops the iterating ~~initialization~~ cycle upon receiving an external "STOP" command on the synchronous SDRAM compatible memory interface, and where the iterating cycle iterates two or more times and performs a power up initialization of the synchronous Flash memory device during each iteration.

16. (Currently Amended) A Flash memory device comprising:

a memory array;

a control circuit; and

a memory interface, wherein the Flash memory device begins a continuously looping ~~initialization~~ cycle upon a power signal on a power bus reaching a specified trip point, and stops the continuously looping ~~iterating initialization~~ cycle upon receiving an external "STOP" command, and where the continuously looping cycle loops at least twice and performs a power up initialization of the Flash memory device during each loop.

17. (Currently Amended) A method of initializing a synchronous Flash memory device comprising:

commencing a continuously looping ~~initialization~~ cycle upon receiving a power signal, where the continuously looping cycle loops at least twice and performs a power up initialization of the synchronous Flash memory device during each loop; and

stopping the continuously looping ~~initialization~~ cycle upon receiving an external system command.

18. (Currently Amended) The method of claim 17, wherein commencing the continuously looping ~~initialization~~ cycle of power up initializations upon receiving the power signal further comprises commencing the continuously looping ~~initialization~~ cycle upon the received power signal reaching a predetermined value.

19. (Currently Amended) The method of claim 17, wherein commencing the continuously looping ~~initialization~~ cycle of power up initializations upon receiving the power signal further comprises commencing the continuously looping ~~initialization~~ cycle upon the received power signal reaching a predetermined value and waiting for a delay period.

20. (Currently Amended) The method of claim 17, wherein stopping the continuously looping ~~initialization~~ cycle of power up initializations upon receiving the external system command further comprises stopping the continuously looping ~~initialization~~ cycle at an in-progress point in the initialization cycle upon receiving the external system command.

21. (Currently Amended) The method of claim 17, wherein receiving the external system command further comprises receiving the external system command through a synchronous interface as one of a hardware signal or a memory software command.

22. (Currently Amended) A method of initializing a memory device comprising:
starting a repeating initialization cycle upon receiving a power signal on a power distribution line, wherein the repeating initialization cycle repeats at least twice and performs a power up initialization of the memory device during each repetition; and
stopping the repeating initialization cycle upon receiving an external system command.

23. (original) The method of claim 22, wherein starting the repeating initialization cycle upon receiving the power signal on the power distribution line further comprises starting the repeating initialization cycle upon the power signal on the power distribution line reaching a predetermined voltage level.

24. (original) The method of claim 22, wherein starting the repeating initialization cycle upon receiving the power signal on the power distribution line further comprises starting the repeating initialization cycle upon the power signal on the power distribution line reaching a predetermined voltage level and waiting a set delay time period.

25. (Currently Amended) The method of claim 22, wherein stopping the repeating initialization cycle upon receiving the external command further comprises stopping the repeating initialization cycle at a random point in the initialization cycle upon receiving the external system command.

26. (original) The method of claim 22, wherein the memory device is a non-volatile memory device.

27. (original) The method of claim 26, wherein the non-volatile memory device is a synchronous Flash memory device.

28. (Currently Amended) A system comprising:
a host controller; and
a synchronous Flash memory device coupled to the host controller, wherein the synchronous Flash memory device comprises,
a memory array,
a control circuit, and
a synchronous memory interface, wherein the synchronous Flash memory device begins an iterating process ~~initialization cycle~~ upon receiving a power signal on a power bus, and stops the iterating process ~~initialization cycle~~ upon receiving an external system command, where the iterating process iterates at least twice and performs a power up initialization cycle of the memory device during each iteration.

29. (original) The computer system of claim 28, further comprising a separate external data source.

30. (original) The computer system of claim 29, wherein the separate external data source further comprises a non-volatile memory device.

31. (original) The computer system of claim 29, wherein the separate external data source is coupled to the host controller on a separate bus.

32. (original) The computer system of claim 31, wherein the separate bus is a non-synchronous bus.

33. (original) The computer system of claim 28, wherein the host controller receives software routines to control the synchronous Flash memory device from a non-volatile data source.

34. (Previously Presented) The computer system of claim 33, wherein the non-volatile data source is a non-volatile memory device containing BIOS.

35. (Currently Amended) The computer system of claim 28, wherein the host controller stops the iterating process ~~initialization cycle~~ of the synchronous Flash memory by issuing the external system command.

36. (original) The computer system of claim 28, wherein the host controller comprises a processor or an integrated chipset.

37. (Currently Amended) A computer system comprising:
a host controller; and
a memory device coupled to the host controller, wherein the memory device begins to iterate a repeating ~~an~~ initialization cycle in response to Vcc, and stops iterating the initialization cycle in response to the host controller, wherein the initialization cycle repeats at least twice and performs a power up initialization of the memory device during each iteration.

38. (Currently Amended) A method of operating a computer system comprising:

coupling a host controller to a memory device;

detecting Vcc in the memory device;

starting an iterating process ~~initialization cycle~~ in the memory device, wherein the iterating process iterates at least twice and performs a power up initialization cycle of the memory device during each iteration; and

stopping iteration of the iterating initialization cycle process in the memory device in response to a software command from the host controller.